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PTO/SB/08A (10-01)
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Substitution for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
Application Number				09/597,076	
Filing Date				January 20, 2000	
First Named Inventor				Yuanning Chen	
Art Unit				2813	
Examiner Name				Kielin, Erik S.	
Attorney Docket Number				CHEN 4-17-157	
Sheet	3	of	5		

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Examiner Signature	<i>E. K.</i>	Date Considered	11/12/02
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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	09/597,076
		Filing Date	January 20, 2000
		First Named Inventor	Yuanming Chen
		Group Art Unit	2813
		Examiner Name	Kielin, Erik S.
		Attorney Docket Number	CHEN 4-17-157
Sheet	4	of	5

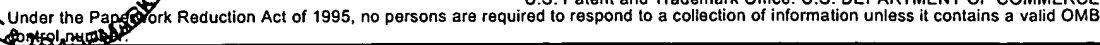
OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue, number(s), publisher, city and/or country where published	T ²
		Ponomarev et al.; High-Performance Deep-Submicron CMOS Technologies with Polycrystalline-SiGe Gates; IEEE Transactions on Electron Devices, Vol. 47, No. 4; April 2000; pp. 848-855.	
		Lee et al.; Enhancement of PMOS Device Performance with Poly SiGe Gate; IEEE Electron Device Letters, Vol. 20, No. 5; May 1999; pp. 232-234.	
		Song et al.; Ultra Thin (<20) CVD Si3N4 Gate Dielectric for Song et al.; Ultra Thin (<20) CVD Si3N4 Gate Dielectric for Deep-Sub-Micron CMOS Devices; Microelectronics Research Center, The University of Texas, Austin; 4 pgs.	
		Hattangady et al.; Ultrathin nitrogen-profile engineered gate dielectric films; Semiconductor Process and Device Center, Texas Instruments; 4 pgs.	
		Tseng et al.; Reduced Gate Leakage Current and Boron Penetration of 0.18 m 1.5 V MOSFETs Using Integrated RTCVD Oxynitride Gate Dielectric; 4 pgs.	
		Hattangady et al.; Remote Plasma Nitrided Oxides for Ultrathin Gate Dielectric Applications; SPIE 1998 Symp. Microelec. Manf.; September 1998; Santa Clara, CA; pp. 1-11.	
		Wu et al.; Improvement of Gate Dielectric Reliability for p+ Poly MOS Devices Using Remote PECVD Top Nitride Deposition on Thin Gate Oxides; IEEE 98 36th Annual International Reliability Physics Symposium; Reno, Nevada; 1998; pp. 70-73.	
		Chatterjee et al.; Sub-100nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process; Semiconductor Process and Device Center, Texas Instruments; 1997 IEEE; 4 pgs.	
		Kraft et al.; Surface nitridation of silicon dioxide with a high-density nitrogen plasma; J. Vac. Sci. Technol. B, Vol. 15, No. 4; 1997 American Vacuum Society; July/August 1997; pp. 967-970.	
		Jeon et al.; Low Temperature Preparation of SiO2 Films With Low Interface Trap Density Using ECR Diffusion and ECR CVD Methods; 1996 Conference on Optoelectronic and Microelectronic Materials and Devices Proceedings, Canberra, ACT, Australia, 8-11 December 1996; pp. 259-262.	
		Rau et al.; Characterization of stacked gate oxides by electron holography; Appl. Phys. Lett., Vol. 68, No. 24; 1996 American Institute of Physics; 10 June 1996; pp. 3410-3412.	

Examiner Signature		Date Considered	11/12/02
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Filing Date	January 20, 2000
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First Named Inventor	Yuanning Chen
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Group Art Unit	2813
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Examiner Name	Kjelin, Erik S.
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Attorney Docket Number	CHEN 4-17-157
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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

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